REMARKS

Claims 1-16 are now pending in the application.

Applicant amends claim 3 to correct a minor antecedent basis error (not noted by the Examiner), and claims 2, 3 and 9 to correct a minor typographical error (also not noted by the Examiner). These amendments to claims 2, 3 and 9 do not change the scope of these claims. No estoppel is created.

The Examiner rejects:

- claims 1, 2, 6, 7 and 12-14 under 35 U.S.C. §103(a) as being unpatentable over JP 07-134277 to Asada (Asada '277) in view of JP 10-334685 to Kanba (Kanba '685);[1]
- claims 3, 5, 8-11, 15 and 16 under 35 U.S.C. §103(a) as being unpatentable over Asada '277 in view of Kanba '685 and further in view of JP 10-74062 to Kihara (Kihara '062); and
- claims 3, 5, 8-11, 15 and 16 under 35 U.S.C. §103(a) as being unpatentable over Asada '277 in view of Kanba '685 and further in view of JP 05-35213 to Asada (Asada '213).

Applicant respectfully traverses the Examiner's rejections as follows.

Applicant's invention provides scanning circuits comprising unique combinations of features including, *inter alia*, at least one delay circuit which delays control clocks supplied to transfer gates relative to control clocks supplied to a feedback circuit (see Applicant's independent claims 1-3, 8 and 9). As explained in Applicant's specification, one of the

[1] Applicant notes that claims 7 and 14 depend from claim 3 which the Examiner does not reject based on Asada '277 and Kanba '685 only. It appears that the Examiner intended to reject claims 7 and 14 based on the combination of references applied against claim 3. Applicant responds accordingly.

drawbacks of the prior art scanning circuits (as shown in Applicant's Fig 7) is that the operational margin for the phase deviation between the control clocks is very low. Applicant's invention is based upon Applicant's recognition that, delaying operation of the timing of the transfer gates, which transfer the start pulse, relative to the operation timing of the feedback circuit, provides a scanning circuit which may have a higher operation margin for the phase deviation between the clock signals so that it may, but is not required to, achieve a more stable operation (see Applicant's specification at, for example, pages 11-13).

Asada '277, the Examiner's primary reference, is described in the "Background of the Invention" section of Applicant's specification, and discloses a scanning circuit and a driving method illustrated in Applicant's prior art Fig. 7 (see Applicant's specification, page 2). The Examiner acknowledges that Asada '277 does not disclose the feature of a delay circuit which delays control clocks supplied to transfer gates relative to control clocks supplied to a feedback circuit, as recited in Applicant's independent claims 1-3, 8 and 9, and relies on Kanba '685 as allegedly supplying this feature.

Kanba '685 discloses a shift register where input of the clock signal to a flip-flop circuit 15 is delayed from that of a latch circuit 16 by means of a delay circuit 19 (see Id., Abstract). The Examiner alleges that latch circuit 16 of Kanba '685 corresponds to a "feedback circuit," and that, therefore, it would have been obvious for one of ordinary skill in the art to "use a delay circuit in delaying the control clock supplied to a feedback circuit in a shift register as taught by Kanba '685 in the device of Asada '277 so as to prevent malfunction and stabilize the operation of the system" (see Office Action, paragraphs 2-4). Applicant respectfully disagrees.

It is only Applicant's own disclosure which recognizes the drawbacks of a scanning circuit as disclosed by Asada '277 (i.e., the drawbacks of operational margin for the phase deviation between the control clocks being very low), and further recognizes that delaying operation of the timing of the transfer gates would provide a scanning circuit which could have a higher operational margin for the phase deviation between the clock signals. Applicant respectfully submits that providing a delay circuit to prevent racing of a shift register device which has latch circuits has nothing to do with delaying operation of control clocks supplied to transfer gates of a scanning circuit, as recited in Applicant's independent claims 1-3, 8 and 9. None of the cited prior art references teaches or suggests such a modification of a scanning circuit discloses by Asada '277.

The following technical assessment of the cited prior art is provided to further clarify some of the differences between Applicant's claimed invention and the cited prior art.

In a circuit according to Asada '277, the scanning circuit outputs scanning pulse signals with the circuit constitution for delay transferring data signals in synchronism with clock signals. The scanning circuit comprises path transistors which are connected in cascade, receive data signals outputted from a preceding stage and output signals as input signal to a next stage to be controlled by one clock signal or a couple of clock signals with mutually inverted relation, feedback circuits which individually receive branch outputted signals from the path transistors by clock signals, compensate for signal level reduction and output, and output buffer circuits which individually receive sequentially outputted signals from the feedback circuits and output as scanning.

In a circuit according to Kanba '685, a plurality of data holding circuits are serially connected and a shift register unit is provided such that the operation of flip-flop circuits and the latch circuit corresponding with the clock signal have opposite logic in the data holding circuit of odd stages and even stages. Kanba '685 discloses a circuit comprising operational delay means which delays the operational timing of the flip-flop circuits over the operational timing of the latch circuit in the data holding circuit.

In a circuit according to Kihara '062, on the basis of first and second clock signals having mutually opposite polarity and being supplied respectively to even and odd stages, there is provided a bi-directional shift register in which left or right directional shift starts when a starting pulse is supplied to the right or left end. The first and second clock signals are supplied to one side of inputs of first and second exclusive OR gates. The shift direction switching signal is added to the other side of inputs of the first and second exclusive OR gates. The output of the first and second exclusive OR gates are supplied to even and odd stages as inverted/non-inverted signals of the first and second clock signals by changing high/low level of the shift direction switching signal.

In contradistinction to Applicant's claimed invention, and as acknowledged by the Examiner, Asada '277 does not disclose, teach or suggest a scanning circuit which adds a delay circuit to a bi-directional shift register.

In Kanba '685, shift register determines the data transmitting direction uni-directionally and clearly differs from bi-directional shifting. That is, in the shift register of Kanba '685, the

clock to control the flip-flop circuit and the clock to control the latch circuit have the same clock line. However, according to an aspect of Applicant's invention, a bi-directional shift register controls the shift direction by the inversion of the phase of a two phase clock which controls the feedback circuit. It would be impossible to control the shifting direction when the clock to control the transmitting portion and the clock to control the feedback circuit have the same clock line as disclosed in Kanba '685. That is, according to an aspect of Applicant's invention, the clock which controls the transmitting portion in the bi-directional shift register and the clock which controls the feedback circuit have an independently different line, respectively. Clearly, such an arrangement is not contemplated in the controlling method of Kanba '685 circuit.

In the structure of shift register according to Kanba '685, plural pairs in which a serial circuit of a transmitting portion (flip-flop circuit) and latch portion is formed are serially connected. According to an aspect of Applicant's invention, a feedback circuit to generate a waveform is connected to a connecting node between transfer gates connected serially. Consequently, according to an aspect of Applicant's invention, the structure of the shift register differs from that disclosed in Kanba '685. In Kanba '685, flip-flop circuit operates as a shift register in serial connection. However, a circuit, according to an aspect of Applicant's invention, does not operate as a shift register because the transfer gates which constitute transmitting portion are serially connected. Applicant respectfully submits that, contrary to the Examiner's analysis, one of ordinary skill in the art of scanning circuits, would readily appreciate that the flip-flop circuit of Kanba '685 does not correspond to a transmitting portion, and the latch circuit of Kanba '685 does not correspond to the feedback circuit, of Applicant's invention. Kanba '685

provides a delay circuit in every flip-flop circuit and latch circuit which constructs its shift register. In contrast, according to an aspect of Applicant's invention, a delay circuit is configured for a signal line which controls the feedback circuit.

Kihara '062 discloses a circuit for addressing the problem of a shift operation not starting when the shift direction is changed. In this regard, Kihara '062 discloses a circuit which changes the shifting direction according to the selection between transfer gate (TRR) and transfer gate (TRL) by shift direction changing signal (CHN). In contrast, a circuit according to an aspect of Applicant's invention changes the shifting direction by the inversion of the supplying clock of the feedback circuit.

According to Kihara '062, the object of changing the phase of the controlling clock according to CHN resides in phase matching between start pulse (STR, STL) and clock signal (CLK). Applicant respectfully submits that one of ordinary skill in the art of scanning circuits would readily appreciate that if, in a scanning circuit, a circuit according to Kihara '062 were to be somehow applied to a circuit according to Asada '685, such a scanning circuit would not be operable because the clock to control the feedback portion delays the clock to control the transmitting portion.

Thus, in formulating the prior art rejections, the Examiner is relying on Applicant's own disclosure, and as such, is engaging in impermissible use of hindsight.

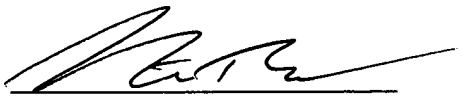
Accordingly, Applicant's independent claims 1-3, 8 and 9, as well as their respective dependent claims 4-7 and 10-16 (which incorporate all the novel and unobvious features of their

base claims) would not have been obvious from any reasonable combination of the cited prior art references.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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